PAPER ID-310868

Subject Code: BEC058

Roll No: | | | | | | | | | | | | |

BTECH
(SEM V) THEORY EXAMINATION 2025-26
CMOS ANALOG VLSI DESIGN

TIME: 3 HRS **M.MARKS: 70**

Note: Attempt all Sections. In case of any missing data; choose suitably.

SECTION A

1. Attempt *all* questions in brief. **02 x 7 = 14**

Q no.	Question	CO	Level
a.	Define threshold voltage of a MOSFET. Mention any two factors affecting it.	1	K2
b.	What is channel length modulation?	1	K2
c.	State the function of a current mirror in analog circuits.	2	K2
d.	Differentiate between thermal noise and flicker noise.	3	K2
e.	What is the Miller effect in CMOS amplifiers?	2	K2
f.	Define gain bandwidth product (GBW) of an op-amp.	4	K2
g.	What is meant by layout versus schematic (LVS) check?	5	K2

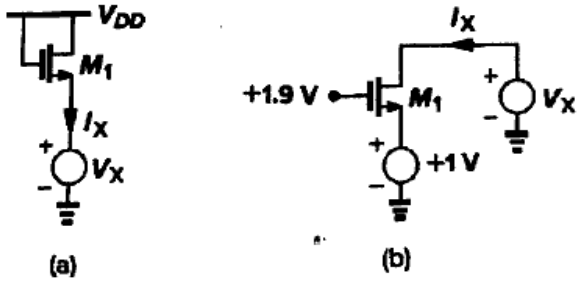
SECTION B

2. Attempt any *three* of the following: **07 x 3 = 21**

a.	Explain briefly about MOS Transconductance with proper expression and diagram	1	K2
b.	Explain the approximate analysis of small signal active pair current mirror circuit.	2	K2
c.	Discuss the noise effect in single stage common source amplifier.	3	K3
d.	Discuss the effect of feedback on noise.	4	K3
e.	Write the short notes on phase margin of MOS amplifier.	5	K3

SECTION C

3. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Sketch I_X and the transconductance of the transistor as a function of V_X for each circuit in **Fig. 1** as V_X varies from 0 to V_{DD}. In part (a), assume that V_X varies from 0 to 1.5 V.  **Figure 1**	1	K5
b.	Sketch V_{out} versus V_{in} for the circuits of **Fig. 2.** as V_{in} varies from 0 to V_{DD}. Identify important transition points.	1	K5

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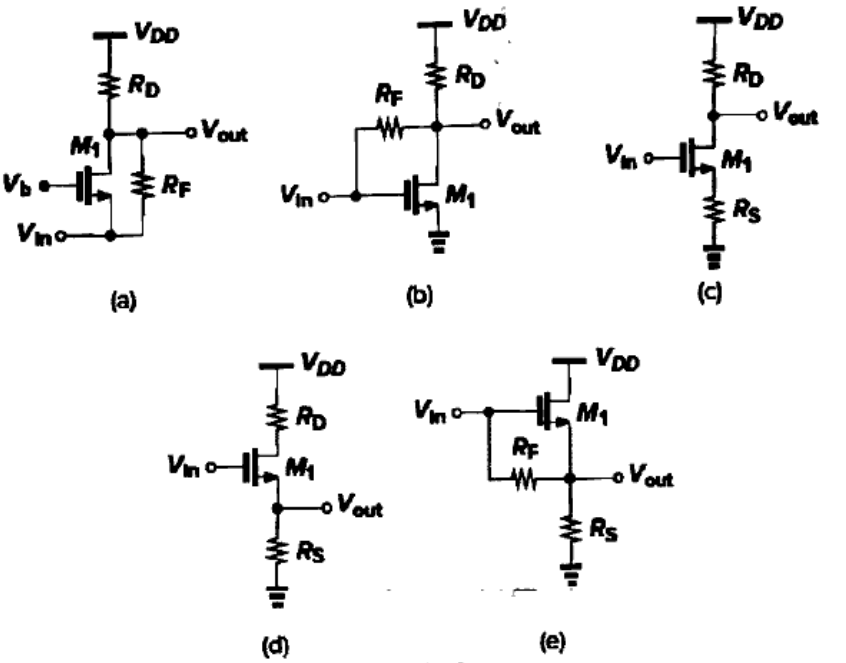

Figure 2

4. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Explain the cascode current mirror circuit with proper expression and diagram	2	K2
b.	In Fig. 3, assume that $(W/L)_1$ = 50/0.5, λ = 0, I_{out} = 0.5 mA, and M1 is saturated. (a) Determine R_2/R_1. (b) Calculate the sensitivity of I_{out} to V_{DD}, defined as $\partial I_{out}/\partial V_{DD}$ and normalized to I_{out}. (c) How much does I_{out} change if V_{TH} changes by 50 mV? (d) If the temperature dependence of μ_n is expressed as $\mu_n \propto T^{-3/2}$ but V_{TH} is independent of temperature, how much does I_{out} vary if T changes from 300°K to 370°K? (e) What is the worst-case change in I_{out} if V_{DD} changes by 10%, V_{TH} changes by 50 mV, and T changes from 300° K to 370°K?	2	K5

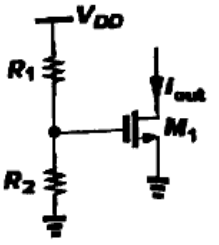

Figure. 3

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5. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Explain the concept of noise power trade-off.	3	K2
b.	Explain the concept of loading in Current voltage Feedback.	3	K3

6. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Explain folded cascode and telescopic op-amp architectures. Compare them in terms of gain, swing, and power dissipation.	4	K2
b.	Explain the concept of gain boosting in MOS Op-amp.	4	K2

7. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Explain the concept of slewing in two stage amplifiers.	5	K2
b.	Study the closed-loop stability if $H(s) = A0/[(1 + s/\omega_{p1})(1 + s/\omega_{p2})(1 + s/\omega_{p3})]$.	5	K5