Printed Pages:01 **Sub Code:REC702**

Paper Id: 231958 **Roll No.** | | | | | | | | | | |

B. TECH
(SEM VII) THEORY EXAMINATION 2022-23
VLSI DESIGN

Time: 3 Hours ***Total Marks: 70***

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt*all* questions in brief. **2x7 = 14**

(a) Define the term testing.
(b) What is a transient response of a circuit?
(c) Discuss the impact of interconnects over VLSI Design.
(d) What are semiconductor memories?
(e) Describe the term fault Models.
(f) Describe the term non-volatile memories.
(g) Explain the term power consumption.

SECTION B

2. Attempt any *three* of the following: **7x3 = 21**

(a) Describe each arm of the Y-Chart with all the points associated.
(b) Explain the calculation process of Logical Effort for the interconnect paths.
(c) Elaborate different techniques used for Energy-Delay optimization in VLSI circuits.
(d) Discuss the term Charge Sharing and explain its avoidance with respect to Domino circuits.
(e) Illustrate different Scan based testing techniques of VLSI circuits.

SECTION C

3. Attempt any *one* part of the following: **7x1 = 7**

(a) Design a 3-input NOR gate using CMOS Logic.
(b) With a neat diagram, Design a Layout of 3-input CMOS NAND gate.

4. Attempt any *one* part of the following: **7x1 = 7**

(a) Describe different causes and avoidance for Static Power Dissipation.
(b) Explain the R-C Delay model for VLSI circuits.

5. Attempt any *one* part of the following: **7x1 = 7**

(a) Discuss the term Interconnect Modelling and explain the sources of resistance present in interconnects.
(b) Calculate Logical Effort of a CMOS inverter circuit.

6. Attempt any *one* part of the following: **7x1 = 7**

(a) Describe the circuit and working of an SRAM cell.
(b) Explain the circuit and working of an EPROM cell.

7. Attempt any *one* part of the following: **7x1 = 7**

(a) Discuss a low-power architecture for any circuit using Voltage Scaling.
(b) Illustrate different Fault Types associated in VLSI Design.